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HP References in this Manual

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4. What measurements will this instrument be used to make? _____

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User's Guide

Publication Number E2455-97006
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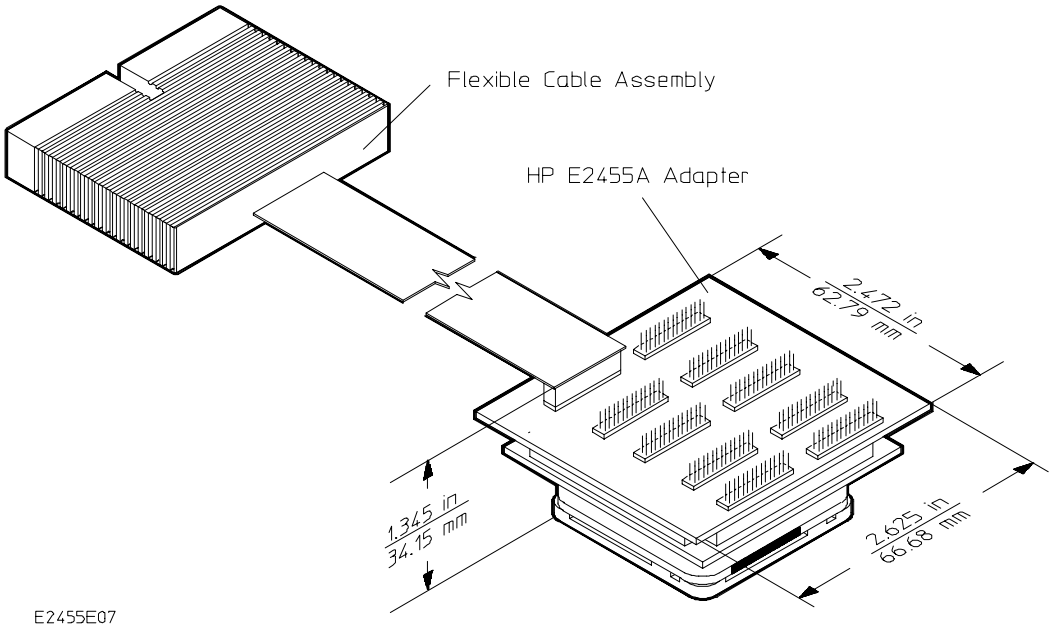
For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2455A PowerPC 603 Preprocessor Interface

The HP E2455A Preprocessor Interface—At a Glance

The HP E2455A Preprocessor Interface provides a complete interface for state or timing analysis between any PowerPC 603 target system and the following HP logic analyzers:

- HP 1660A/AS/C/CS
- HP 1670A
- HP 16550A (two cards)
- HP 16554A (two or three cards)
- HP 16555A (two or three cards)
- HP 16556A (two or three cards)



HP E2455A Preprocessor Interface

In This Book

This book is the user's guide for the HP E2455A Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters:

Chapter 1 explains how to attach the preprocessor to the target and how to configure the logic analyzer for state and/or timing analysis.

Chapter 2 provides reference information on the format specification and symbols configured by the preprocessor interface software and information about the inverse assemblers and status encoding.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

Contents

1

Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the HP E2455A Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers.

This section lists the logic analyzer(s) supported by the HP E2455A and provides other information about the analyzer(s) and the preprocessor interface.

Equipment Supplied

- The preprocessor interface, including the HP E5315A PQFP probe adapter, the HP E2455-66501 PowerPC 603 interface card, and flexible cables.
- The installation kit.
- The configuration files, inverse assemblers, and HP 16505A Prototype Analyzer software on three 3.5-inch disks.
- This User's Guide.

Minimum Equipment Required

- The HP E2455A preprocessor interface.
- The configuration and inverse assembler software on 3.5-inch disks.
- One of the logic analyzers listed in the following table:

Table 1-1 Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16550A (two cards)	204	100 MHz	250 MHz	4 k states
16555A (two cards)	136	110 MHz	250 MHz	1 M states
16555A (three cards)	204	110 MHz	250 MHz	1 M states
1660A/AS/C/CS	136	100 MHz	250 MHz	4 k states
16554A (two cards)	136	70 MHz	125 MHz	500k states
16554A (three cards)	204	70 MHz	125 MHz	500k states
16556A (two cards)	136	100 MHz	200 MHz	1M states
16556A (three cards)	204	100 MHz	200 MHz	1M states
1670A	136	70 MHz	125 MHz	64k states

Optional	Software Version
HP 16505A Prototype Analyzer	A.01.22 or higher

Setting Up the Preprocessor Interface Hardware

Setting up the preprocessor interface hardware consists of the following major steps:

1. Turn off the logic analyzer and the target system.
2. Separate the probe adapter assembly and the interface card.
3. Prepare to attach the locator base to the target system.
4. Test the alignment before adhering the locator base.
5. Adhere the locator base to the target system.
6. Install the probe adapter assembly on the locator base.
7. Reattach the interface card to the probe adapter assembly.

The remainder of this section describes these general steps in more detail.

Turn off the logic analyzer and the target system

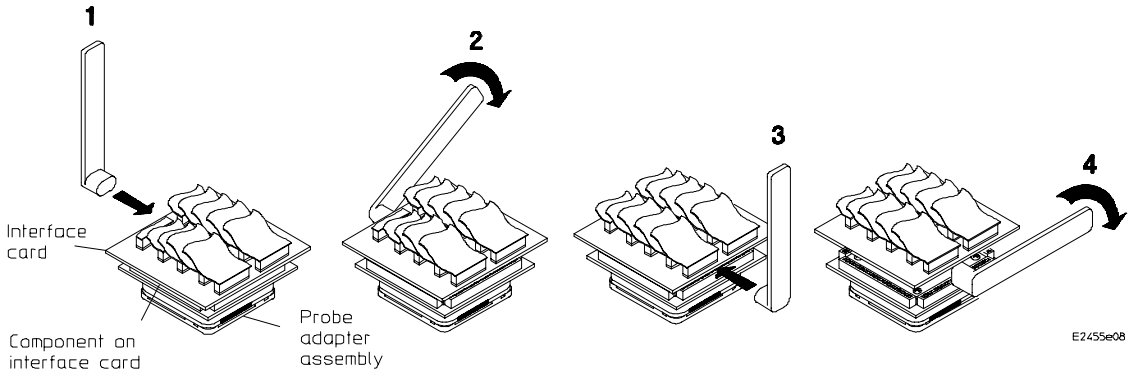
To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. The logic analyzer should always be powered up before the target system. When powering down, power down the target system first and then power down the logic analyzer.

Separate the probe adapter assembly from the interface card

- Gently pry the interface card from the probe adapter assembly using the pry tool as shown.

CAUTION

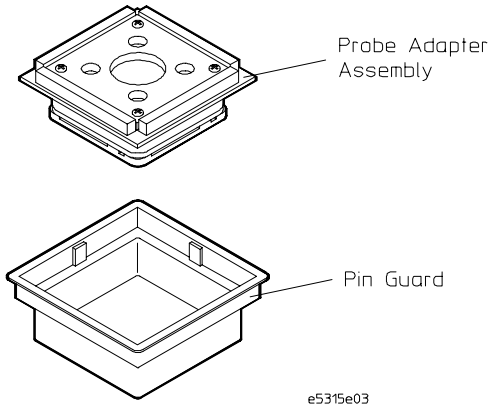
There are components on two sides of the interface card. Do not pry from those sides.



Probe Adapter Removal Diagram

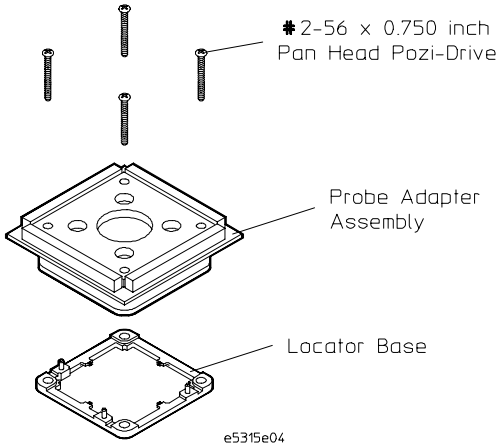
Prepare to attach the locator base to the target system

1 Remove the pin guard. During storage of the probe, put the pin guard back on to protect the pins from damage.



Adapter Preparation I Diagram

2 Unscrew the four screws and remove the locator base.



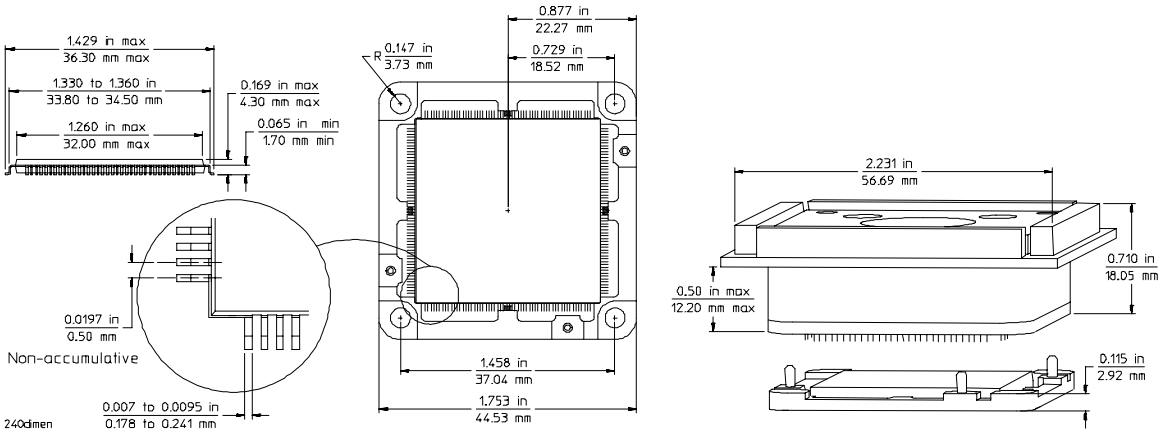
Adapter Preparation II Diagram

3 Check the area around the package to be probed. The minimum required clearance from the package to be probed and any surface-mounted components is 6 millimeters or 0.236 inches.

The probe will work within the parameters shown in the dimension diagram below. Any dimensions outside of this window may require special adjustments in probe positioning for it to be operational.

CAUTION

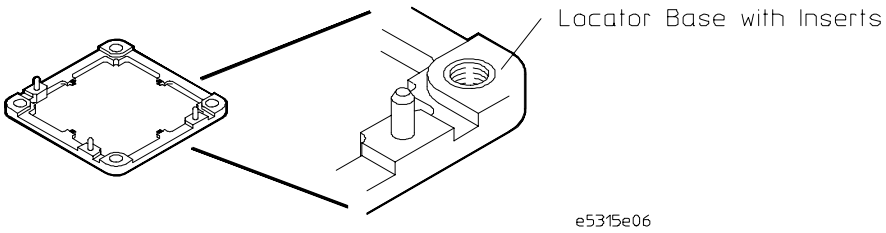
Use grounded wrist straps and mats when installing or performing any service to your probe adapter. Electrostatic discharge can damage electronic components.



Dimension Diagram

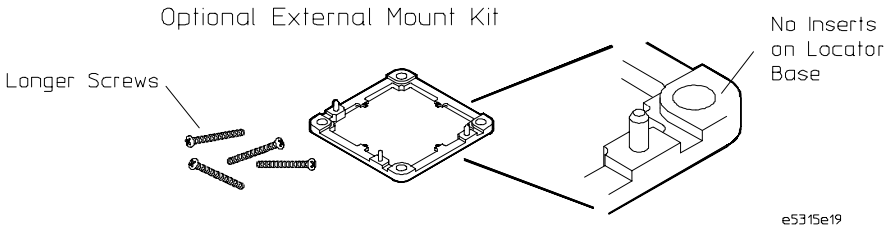
4 Use the locator base provided or mount inserts on your PC board.

If you are using the locator base provided, it has inserts mounted in the corners for use on PC boards that do not have mounting holes laid out to accept a locator base. For probing additional ICs, refer to Table 3-2 for locator kit part numbers.



Locator Base with Inserts Diagram

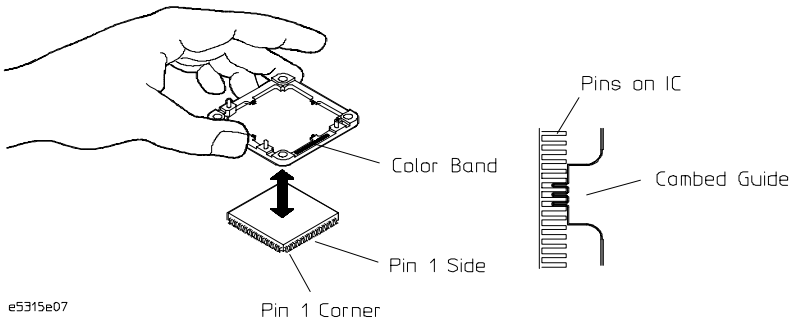
If you are mounting inserts on your PC board, then use an external mount kit which has a locator base without inserts and longer screws. The external mount kit is HP part number 5041-9490. It is not included with the preprocessor, and must be ordered separately. The locator base without inserts does not need to be glued down. Refer to the dimension diagram on the previous page to layout and mount four #2-56 inserts on your PC board.



External Mount Kit Diagram

Test the alignment before adhering the locator base

1. Remove any flash at the corners of the IC or between pins which will inhibit the locator base seating on the board.
2. Align the color band on the locator base with the Pin 1 side of your package as shown in the following diagram.
3. Place the locator base on the package to be probed to see that it is located properly. The combed guides on all four sides must be centered on the package sides and seated on the board.



Alignment Diagram

4. Remove the locator base. You are now ready to adhere the locator base.

Adhere the locator base to the target system

1. Clean the target board to prepare it for applying adhesive.
2. Apply adhesive to the target system using the outline of the locator base as a guide. Follow the manufacturer's recommended temperature parameters for the adhesive (in the Material Safety Data Sheet enclosed).

WARNING

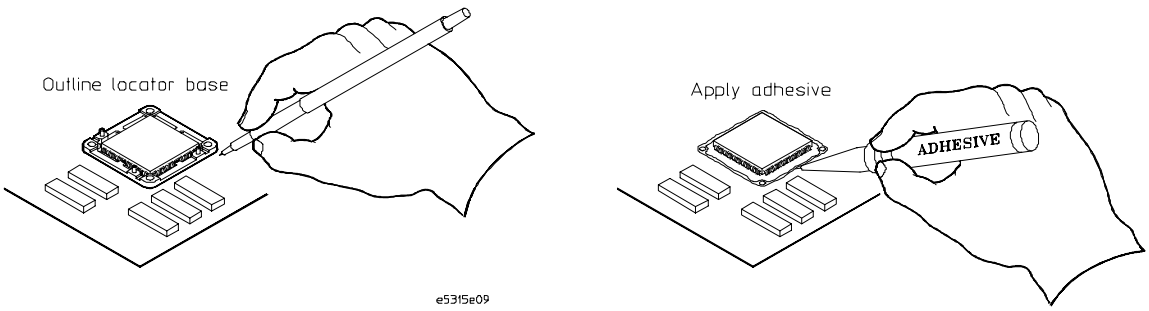
Read the Material Safety Data Sheet enclosed for handling precautions on the Loctite® Superbonder495® or call Loctite Corporation at (203) 571-5100.

Loctite Instant Adhesives are nontoxic. The vapors can cause eye irritation in poorly ventilated areas or low-humidity environments.

Accidental skin bonding is best handled by passive, nonsurgical first aid. Hot soapy water aids separation of skin tissue. Use peeling, not pulling action to separate bonded tissue.

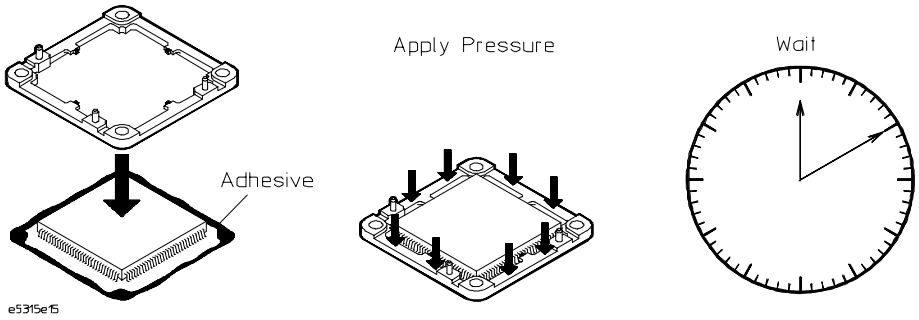
CAUTION

Installation of the locator base to the target system is considered PERMANENT. Any attempt to remove the IC, locator base, or the PC board may result in damage to all three parts.



Adhesive Application Diagram

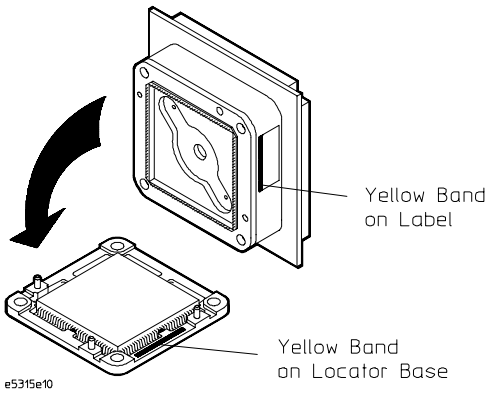
3 Place the locator base back onto the package to be probed and apply downward pressure to ensure that the locator base adheres to the PC board. Allow the adhesive to set at least ten minutes before attaching the probe adapter.



Locator Base Attachment Diagram

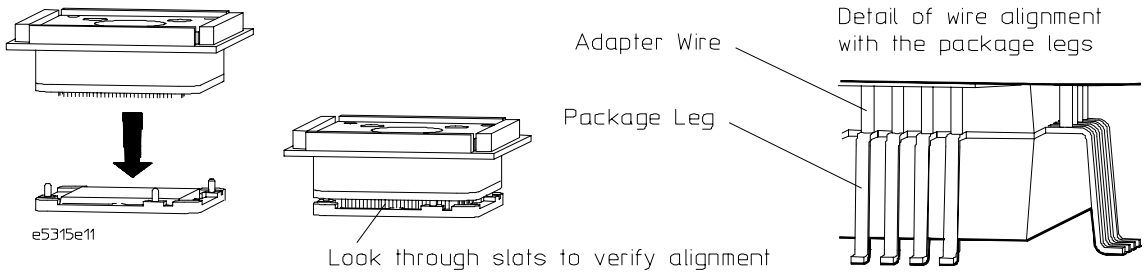
Install the probe adapter assembly on the locator base

1 Align the yellow band on your probe adapter assembly with the yellow band on the locator base.



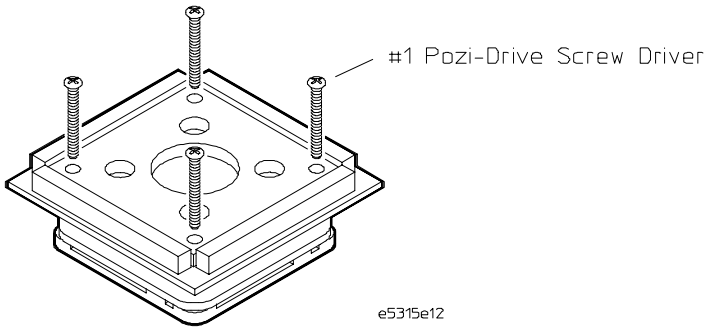
Probe Adapter Alignment I Diagram

2 Slide the adapter down on the pins until the adapter wires touch the package legs. Make sure that the wires align with the package legs around the entire package by using a magnifying glass and light. Every wire must be directly above a leg, or must not be more than one-half of a wire diameter off to one side.



Probe Adapter Alignment II Diagram

3 Insert the four corner mounting screws through the adapter and into the locator base corner inserts. Turn them until the slack is taken up. Then turn each screw a half turn alternating between all four screws in until all screws are snug. Check again to verify that the wires align around the entire package.



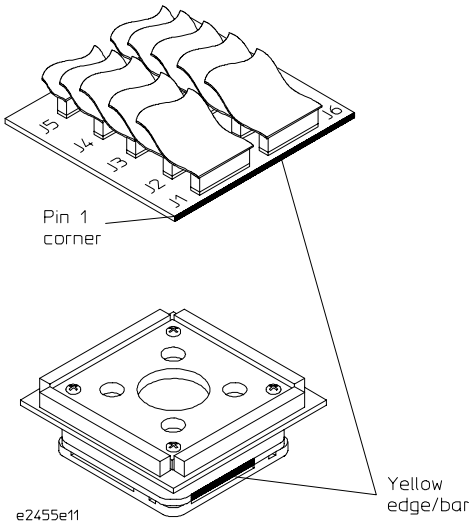
Probe Adapter Alignment III Diagram

Reattach the interface card to the probe adapter assembly

- Align the pin 1 corner of the interface card with the pin 1 corner of the probe adapter, and insert the card into the adapter.

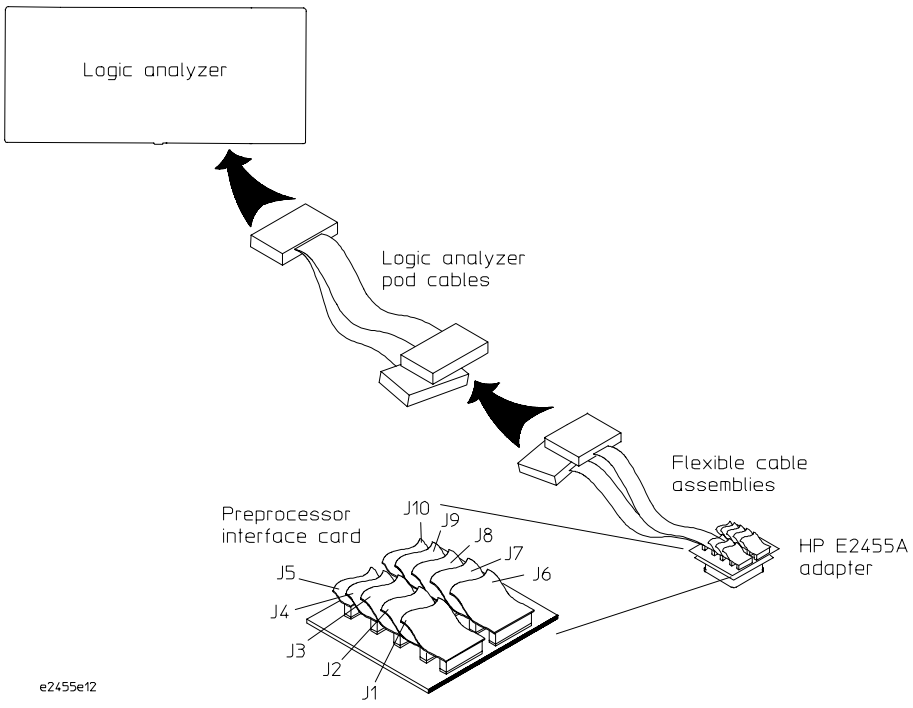
CAUTION

The yellow edge of the interface card must be on the label (yellow bar) side of the probe adapter. Incorrect alignment may cause damage to the microprocessor.



Preprocessor Interface Assembly Diagram

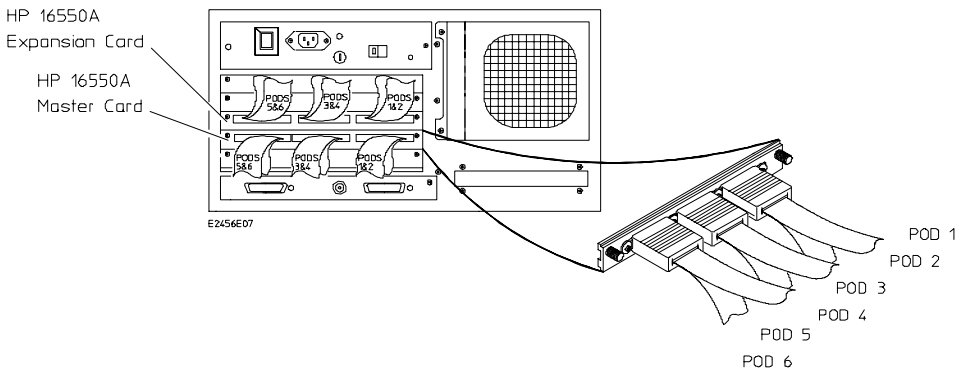
Connect the logic analyzer pod cables to the logic analyzer and to the flexible cable assemblies on the preprocessor interface. Refer to the pod diagram for the analyzer you are using.



Logic Analyzer Hardware Overview Diagram

To connect to the HP 16550A two-card analyzer

- Connect the pod cables to the preprocessor interface according to the pod diagram below.



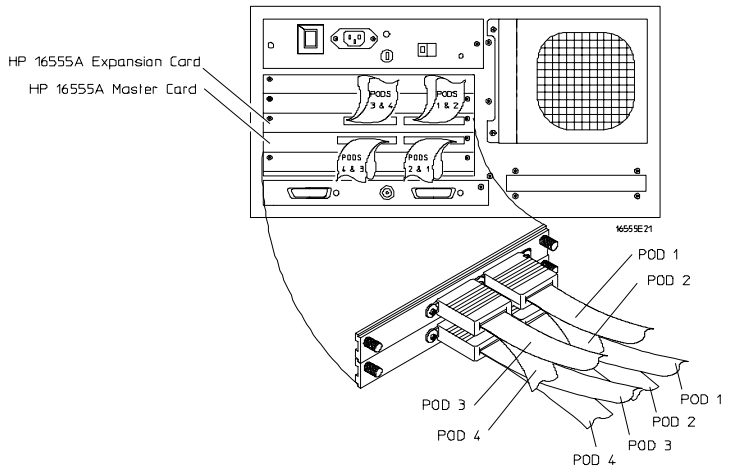
HP 16550A Expansion Card	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2455A Connector	J5 STAT	J2 STAT	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B

HP 16550A Master Card	Pod 6	Pod 5	Pod 4	Pod 3
HP E2455A Connector	J6 misc	J1 misc	J3 ADDR	J4 ADDR clk ↑

Configuration File
Use configuration files C603F and CP603F for the HP 16550A logic analyzer. See Table 1-2.

To connect to the HP 16554A/55A/56A two-card analyzer

- Connect the pod cables to the preprocessor interface according to the pod diagram below.



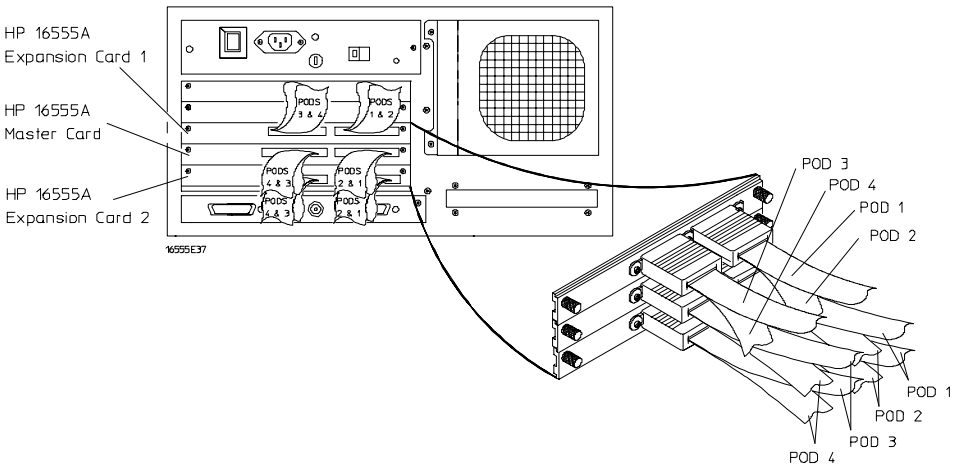
HP 16554A/55A/56A Expansion Card	Pod 4	Pod 3	Pod 2	Pod 1
HP E2455A Connector	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B

HP 16554A/55A/56A Master Card	Pod 4	Pod 3	Pod 2	Pod 1
HP E2455A Connector	J5 STAT	J2 STAT	J3 ADDR	J4 ADDR clk ↑

Configuration File
Use configuration files C603M and CP603M for the two-card HP 16554A/55A/56A. See Table 1-2.

To connect to the HP 16554A/55A/56A three-card analyzer

- Connect the pod cables to the preprocessor interface according to the pod diagram below.

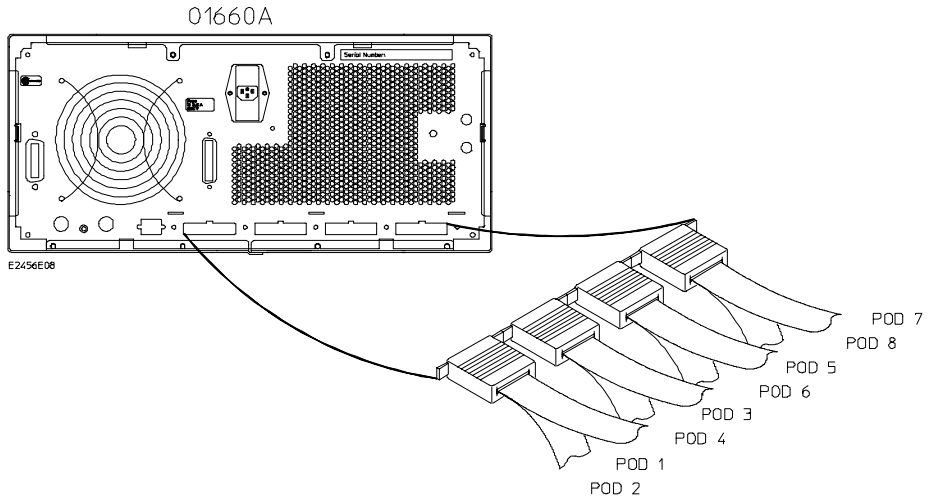


Exp. Card 1	Pod 4	Pod 3	Pod 2	Pod 1
HP E2455A Connector	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B
Master Card	Pod 4	Pod 3	Pod 2	Pod 1
HP E2455A Connector	J6 misc	J1 misc	J3 ADDR	J4 ADDR clk ↑
Exp. Card 2			Pod 2	Pod 1
HP E2455A Connector			J5 STAT	J2 STAT

Configuration File
Use configuration files C603M3 and CP603M3 for the three-card HP 16554A/55A/56A. See Table 1-2.

To connect to the HP 1660A/AS analyzer

- Connect the pod cables to the preprocessor interface according to the pod diagram below.

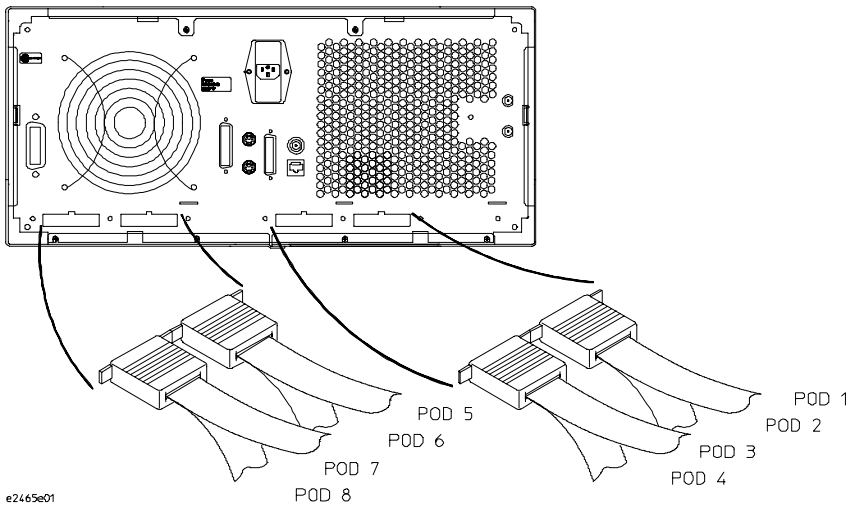


HP 1660A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6	Pod 7	Pod 8
HP E2455A Connector	J4 ADDR clk ↑	J3 ADDR	J8 DATA_B	J10 DATA_B	J7 DATA	J9 DATA	J2 STAT	J5 STAT

Configuration File
Use configuration files C603J and CP603J for the HP 1660A/AS/C/CS logic analyzers. See Table 1-2.

To connect to the HP 1670A logic analyzer

Use the table below to connect the preprocessor to the HP 1670A logic analyzer.



HP 1670A Pod	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2455A Connector	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B	J5 STAT	J2 STAT	J3 ADDR	J4 ADDR clk ↑

Configuration File
Use configuration files C603M and CP603M for the HP 1670A logic analyzer. See Table 1-2.

Loading The Configuration and Inverse Assembler Files

Configuring the logic analyzer consists of loading the software by inserting the floppy disk in the logic analyzer and loading the configuration file. The configuration file you use is determined by the logic analyzer. Note that there are two disks with configuration files (refer to step 1).

To load the configuration and inverse assembler

The first time you set up the preprocessor interface, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers with a hard disk (HP 1670A, HP 1660C/CS, or an analyzer in the HP 16500B frame), you might want to create a directory such as PPC603 on the hard drive and copy the contents of the appropriate floppy (refer to step 1) onto the hard drive. You can then use the hard drive for loading files.

1 **Select the appropriate configuration disk and insert it in the front disk drive of the logic analyzer.**

There are two disks provided for the PowerPC 603. The "Delayed AACK" disk is for target systems in which the memory system delays AACK until the completion of the data phase. The "Pipelining" disk is for target systems which may assert AACK before the completion of the data phase.

2 **Go to the Flexible Disk menu.**

3 Configure the menu to load.

4 Use the knob to select the appropriate configuration file.

Choosing the correct configuration file depends on which logic analyzer you are using. Table 1-2 shows the correct configuration files for each logic analyzer.

5 Select the appropriate analyzer on the menu.

6 Execute the load operation on the menu to load the file into the logic analyzer.

The logic analyzer is configured for PowerPC 603 analysis by loading the appropriate configuration file. Loading this file also automatically loads an inverse assembler.

7 If you want to load a different inverse assembler, repeat steps 2 through 6, selecting the inverse assembler file in step 4. Refer to "Using the Inverse Assembler" in Chapter 2 for information on inverse assemblers.

8 If you are using the HP 16505A Prototype Analyzer, insert the "16505 Prototype Analyzer" flexible disk into disk drive of the prototype analyzer and update the HP 16505A from the Session Manager. You must close your workspace to run the update.

The HP 16505A Prototype Analyzer requires software version A.01.22 or higher to work with the HP E2455A.

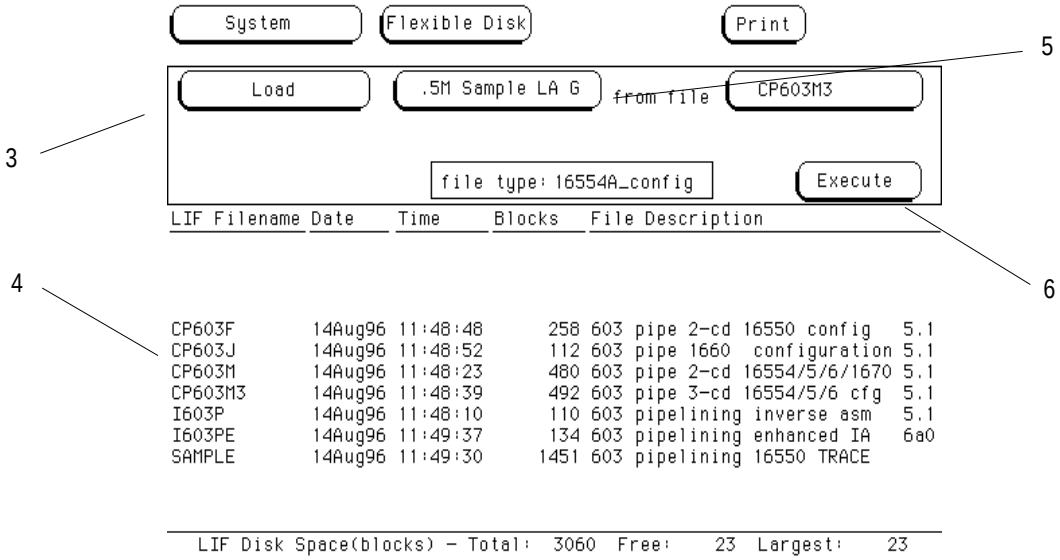


Table 1-2 **Logic Analyzer Configuration Files**

Analyzer Model	Delayed-AACK Configuration File	Pipelined Configuration File
16550A (two cards)	C603F	CP603F
16554A/55A/56A (two cards)	C603M	CP603M
16554A/55A/56A (three cards)	C603M3	CP603M3
1660A/AS/C/CS	C603J	CP603J
1670A	C603M	CP603M

Once you have the hardware and software set up, you are ready to analyze the PowerPC 603 with the logic analyzer and preprocessor interface.

Analyzing the PowerPC 603

Analyzing the PowerPC 603

This chapter describes preprocessor interface data, symbol encodings, and information about the available inverse assemblers.

The PowerPC and logic analyzer use opposite conventions to designate individual signals on a bus. In PowerPC nomenclature, bit 0 is the most significant; in the analyzer, it is the least significant. In PowerPC, A0 is the most significant bit of the address bus; on the analyzer, the most significant bit is called ADDR31.

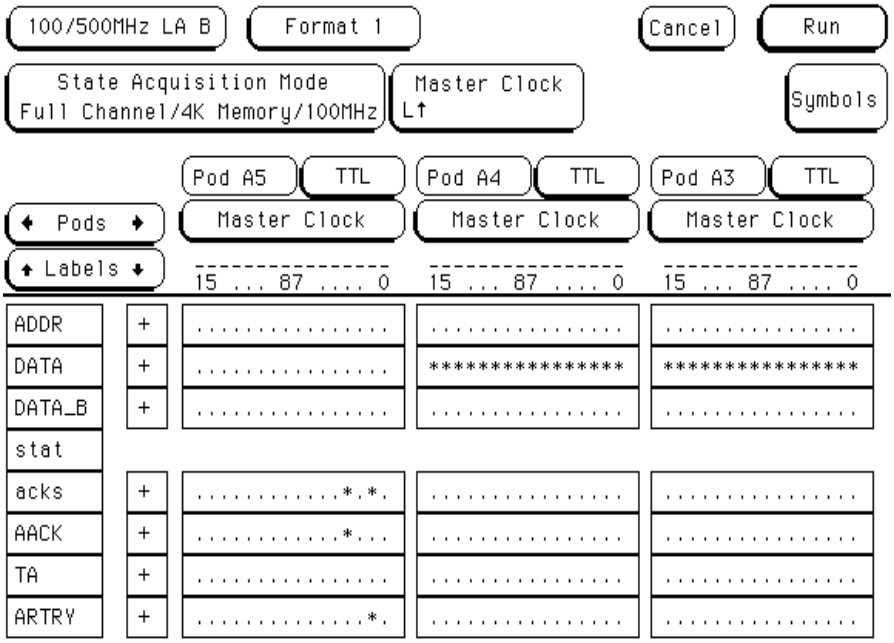
Most Significant	Least Significant	
A0	A31	PowerPC
ADDR31	ADDR0	Analyzer

This may cause confusion in the waveform menus when using Channel Mode Sequential or Individual.

Format Menu

This section describes the organization of PowerPC 603 signals in the logic analyzer's Format Menu.

The configuration software sets up the analyzer format menu to display either eight or ten pods of data, depending on the analyzer. The following figure shows part of the HP 16550 Format Menu.



The following table describes the signals that comprise the analyzer's STAT label. Most of the status and control signals on the PowerPC 603 are active low ("-" suffix). To conserve display space, the "-" is omitted in many of the Format definitions.

The inverse assembler uses STAT bits TC0, TSIZ0...2, TT0...3 , TBST, TA, AACK, ARTRY, DRTRY, ABB, TEA, and TS. Table 3-1 in Chapter 3 lists all the PowerPC 603 signals probed and their corresponding analyzer channels.

Table 2-1 Status Bit Description

Status Bit	Description
BR-	The PowerPC 603 asserts Bus Request to indicate that it has business to conduct on the address bus
BG-	The memory system asserts Bus Grant to allow the 603 onto the address bus
ABB-	Address Bus Busy indicates that the address bus is in use
TS-	The PowerPC 603 asserts TS- for one cycle to commence a transaction. It also serves as the data bus request signal if the TT signals indicate a data transfer.
XATS-	XATS commences a "programmed i/o" (PIO) sequence in the extended address transfer protocol.
DBG-	The memory system asserts Data Bus Grant to allow the 603 onto the data bus.
DBWO-	The memory system may assert Data Bus Write Only to allow the 603 to envelope a data write (snoop push, typically) between the address and data phases of a data read.
DBB-	Indicates Data Bus Busy.
AACK-	The memory system asserts AACK for one cycle to acknowledge an address.
ARTRY-	The memory system may assert ARTRY to cause the 603 to back off the bus and retry the transaction.
TA-	The memory system asserts TA to acknowledge a data transaction.
DRTRY-	The memory system may assert DRTRY to cancel the effect of a TA in the previous cycle.
TEA-	The memory system may assert TEA to indicate a transfer error, e.g. an unmapped part of the address space.
TT 0:3	The Transfer Type signals indicate the direction and purpose of a bus transaction.
Atomic(TT0)	Usually, TT0 asserted indicates an atomic (eg, stwcx.) transfer.
R/-W (TT1)	TT1 is high for a read, low for a write.

Status Bit	Description
InvIdt (TT2)	Usually, the PowerPC 603 asserts TT2 to indicate that the corresponding cache line should be invalidated by other processors.
A Only (TT3)	TT3 high indicates that there is data associated with the current address. TT3 low usually indicates an address-only transaction.
TC 0:1	The Transfer Code outputs provide further information about the current transfer. For a read, they indicate whether instructions or operands are being fetched.
TBST-	When asserted, TBST- indicates a four-beat burst transfer of eight words.
TSIZ 0:2	Indicates the size for the data transfer in conjunction with TBST-.
WT-	Write Through indicates a write-through transaction that should be pushed through local caches to shared memory.
CI-	Cache Inhibit indicates that the 603 will not cache a read.
GBL-	Global indicates the transaction is global, i.e., should be snooped by all other caching devices on the bus.
SRESET-	A falling-edge input causes the 603 to undergo a soft reset.
HRESET-	Input asserted causes the 603 to undergo a hard reset.
CKSTP-	Input asserted causes the 603 to undergo machine check processing.
INT-	Input indicates an external interrupt is pending.
CHECKSTOP	Output indicates that the 603 has entered the machine check state, i.e., stopped.
QREQ-	The PowerPC 603 asserts Quiescent Request to indicate that it wants to be, or is, in a snooze mode.

If you are probing a 603e, the signal labeled XATS- is actually CSE1 (and CSE, on pod J6, is actually CSE0). You may wish to change the name of this label. In the format menu, select the XATS label, and use the Modify Label feature to change the name to CSE1. (DO NOT modify the bit assignments to the STAT label.)

The configuration files also define a number of symbols which make several of the STAT fields easier to interpret. The following table lists the symbol definitions.

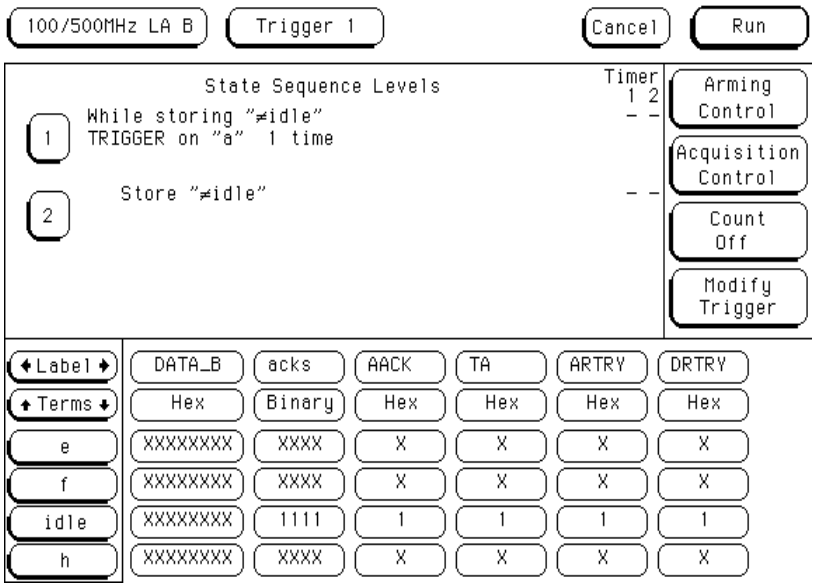
Table 2-2 Symbol Description

Label	Symbol	Encoding
acks	idle	1111
	ARTRY	xxx0
	DRTRY	0xxx
	TA AACK	x00x
	AACK	xx0x
	TA	x0xx
R/-W	rd	1
	wr	0
TSIZ	burst	xxx0
	8 byte	0001
	1 byte	0011
	2 byte	0101
	3 byte	0111
	4 byte	1001
	5?byte	1011
	6?byte	1101
	7?byte	1111
TT	Kill Block	0110
	Wr Graphics	1010
	Rd Graphics	1110
	Clean Block	0000
	Write	0001
	Wr/Kill	0011
	Read	0101
	Rd/Flush	0111
	Wr/Atomic Flush	1001
	Read Atomic	1101
	Rd/Flush Atomic	1111
	?Flush Block	0010
	?DSYNC	0100
	?eieio	1000
	?(reserved)	1011
	?TLB Invalidate	1100
STAT	inst fetch	xxxx xxxx xxxx xxx1 xxxx 1xxx xxxx 0xxx

The least significant bit of the TSIZ label is the TBST- signal. The symbols prefixed by "?" represent signal outputs defined by the PowerPC architecture but not asserted by the PowerPC 603. An instruction fetch is indicated by AACK asserted (address & qualifiers valid), R/-W (TT1) asserted for read, and TC0 asserted.

This section describes some PowerPC 603-specific considerations in triggering the analyzer.

The trigger menu determines what will be acquired by the analyzer and when it will be acquired. The HP E2455A software preconfigures a storage qualification term to exclude wait and idle states from the analyzer's memory. The following figure shows the trigger menu as configured by the HP 16550.



The configuration software renames a pattern term to "idle" and assigns it a pattern with AACK, ARTRY, TA, and DRTRY, all high (de-asserted). The sequencer is programmed to store only states ≠ idle. That is, only states where one or more of these signals is asserted will be stored.

To configure the analyzer to store wait and idle states, change the storage qualification from "≠ idle" to "anystate". Doing so will capture all states (state-per-clock).

To accurately trigger on a specific address, enter the address in the ADDR field of a trigger term and also enter 0 in the AACK field of the term. This will ensure against false triggering on a floating address bus.

The instruction addresses presented on the PowerPC 603 address bus always end in hex 0 or hex 8. When the instruction cache is enabled, the 603 will burst four data beats per address and will not update the address as it bursts. To accurately trigger on the fetch of a particular address when bursting, the least significant five bits of the address should be "don't cares. " Change the base of the ADDR label to Binary to enter the 5 X's.

Using the Inverse Assemblers

This section discusses the general output format of the inverse assemblers and processor-specific information.

To select a different inverse assembler

There are two inverse assemblers provided for each target memory configuration, a generic inverse assembler (I603 or I603P) and an enhanced inverse assembler (I603E or I603PE). The enhanced inverse assembler only works with certain configurations of logic analyzer, frame, and software revision. One of these inverse assemblers is loaded by default when you load the analyzer configuration file.

The generic disassembler provides basic disassembly, with overfetch marking and high/low alignment selection. The enhanced disassembler adds the ability to show or suppress various states from the state listing, and allows you to select mnemonic and numeric display formats.

The generic inverse assembler is loaded automatically on the HP 16500A, and on the HP 1660-series equipment with a revision level lower than 2.00. The generic inverse assembler may be manually loaded on any of the logic analyzers, using the procedure described in chapter 1.

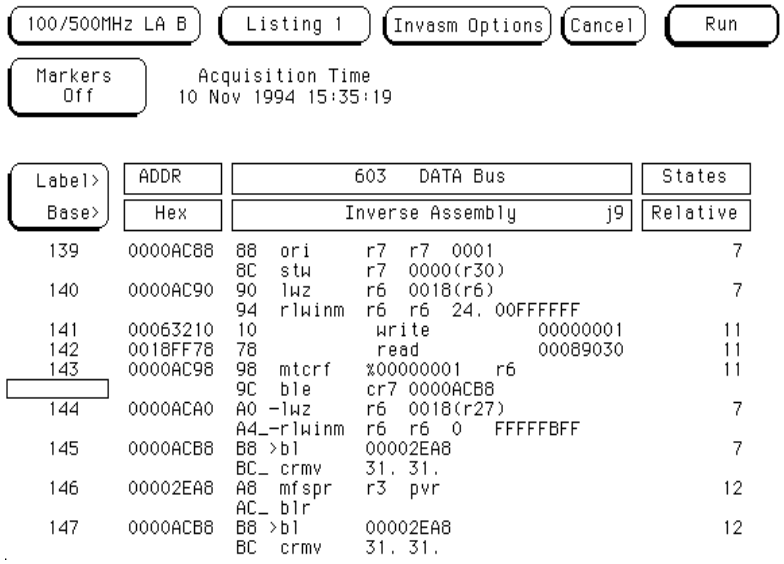
The enhanced inverse assembler is loaded automatically on the HP 16500B and the HP 1670A, and on the HP 1660-series equipment with a software revision of 2.00 or higher. The enhanced inverse assembler may be manually loaded on an HP 16500A running software revision 6.00 or higher.

To load a different inverse assembler, refer to "Loading the Configuration" in Chapter 1.

To display captured state data

Select the Listing Menu for your logic analyzer.

The logic analyzer displays captured state data in the Listing Menu. The inverse assembler display is obtained by setting the base for the DATA label to Invasm. The following figure shows a typical Listing Menu display.



The columns on the left of the inverse assembly display are the least significant hexadecimal digits of an instruction or burst address. These may be useful for matching an execution trace to an assembly listing. Because the PowerPC 603 presents one address and then reads two or eight instructions for each address, the bits are synthesized by the disassembler. On the HP 16505A Prototype Analyzer, the entire synthesized address appears under the label "PC". The actual address bits presented by the 603 may be observed under the ADDR label.

The third column may contain an underscore "_", which indicates a break in the sequential flow of instruction addresses.

The fourth column displays overfetch and branch-and-link indicators as described in the overfetch marking section on page 2-12. The remaining disassembly listing resembles an assembly listing.

Interpreting Data

General purpose registers are displayed as r0, r1, ..., r31. Floating point registers are displayed as f0, f1, ..., f31. Condition registers are displayed as cr0, cr1, ..., cr7. Special purpose registers are displayed using their mnemonic.

Most numerical data is displayed in hexadecimal, e.g.,
"lwz r28 0044(r1)" or
"lwz r28 0x0044(r1)."

Bit numbers and shift counts are displayed in decimal, e.g.,
"cror 31. 31. 31." or
"cror 31 31 31."

A few instructions display some operands in binary, e.g.,
"mtfsfi 4 %0101" or
"mtfsfi 4 0b0101."

The disassembler decodes the full PowerPC instruction set architecture including 64-bit mode instructions and optional instructions not implemented on the 603. When these unimplemented opcodes are encountered, the instruction mnemonic has a "?" prefix. If a reserved bit is set in an instruction opcode field, a "?" is appended most often to the mnemonic, but in some cases to an operand.

An instruction word of 00000000 is decoded as "illegal." Otherwise, if an opcode field is invalid, it is shown as "Undefined Opcode".

Branch Instructions

If the address of a branch relative instruction is known, its target is presented as an absolute hex address (or as a symbol if it matches an ADDR pattern or range symbol). If the address of a branch relative instruction is not known, its target is displayed as a hexadecimal offset such as +00000C30 or -00000048.

If a branch hint is encoded, a "+" (for predicted taken) or a "-" (for predicted not taken) is appended to the conditional branch mnemonic.

Overfetch Marking

Overfetch refers to instructions which are fetched but not executed by the processor. They may arise from the following sources:

- When bursting, the 603 first fetches the critical doubleword of an eight-word cache line. The memory system then provides succeeding doublewords. If the critical doubleword was not the first doubleword of the line, the memory system wraps at the line boundary to the first doubleword. Doublewords fetched after the line wrap are not in the sequential execution path and are marked with an asterisk "*".
- When the 603 executes a branch instruction, the instructions between the branch and the branch target are not executed. These instructions are indicated with a hyphen "-". If the instruction cache is enabled, the branch target may already be in the cache and will not be fetched over the bus. The remaining cache line containing the branch will be marked as overfetch.
  In some cases, the bus trace is ambiguous as to whether or not a conditional branch was taken. In these cases, the possibly-overfetched instructions are marked with an interrogation point "?" instead of a hyphen.

An exception to the above includes branches with the link bit set that record the next instruction address in the link register ("lr"). Frequently, these are subroutine branches which will return to the instructions following the branch. If the instruction cache is enabled, these branch-and-link instructions are indicated by a ">".

Little-Endian Mode

The inverse assembler is designed to support the native big-endian mode of operation on the PowerPC 603. When operating in little-endian mode, the 603 uses a technique known as "address munging" to convert internal little-endian addresses into external big-endian addresses. Internal and external addresses may differ from one another in the three least significant bits.

In little-endian operation, in a given data beat, the instruction word from DL0..31 (DATA_B label; external address xxx4) will be dispatched before the instruction word from DH0..31 (DATA label; external address xxx0). You can compensate for this by exchanging the DATA and DATA_B labels in the Format menu. However, while this will correctly order 32-bit word reads on the 64-bit data bus, it will cause byte- and half- word reads and writes to appear on the opposite side of the bus, and swap the halves of double-word reads and writes.

To use the Invasm key

The disassembler may occasionally mispredict a conditional branch instruction as taken and incorrectly mark subsequent states as overfetch. The following steps may be taken to correct this:

- Roll the first incorrectly marked state to the top of the listing screen and select the Invasm key.
- Select High or Low as the first or second word of the double word that is incorrectly marked.

  Note that the PowerPC 603 may branch to the second word of a doubleword without the disassembler detecting it. This could be a branch from cache or via the lr, ctr, or srr0 registers. If the first word of the target doubleword is a branch, the inverse assembler may incorrectly mark the second word as overfetch.

To use the Invasm Options key

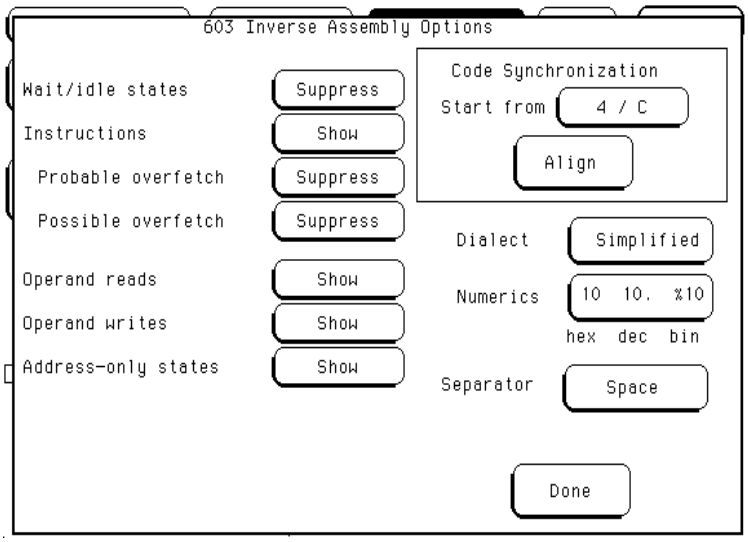
The enhanced inverse assembler contains additional features which use the increased capabilities of some of the logic analyzers. These features are accessed through the Invasm Options menu. Note that all the features in the generic inverse assembler are included in the enhanced inverse assembler (see previous section).

The I68360E Inverse Assembly Options menu contains three functions: display filtering with Show/Suppress selections, Code Synchronization, and Display Options. The following sections describe these functions.

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Show/Suppress

The enhanced inverse assembler (I603E or I603PE) supports selective suppression of certain states in the state listing display. The show/suppress settings do not affect the data that is stored by the logic analyzer; they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements. The figure below shows the states that have the Show/Suppress option.



Suppressing wait/idle states is useful for obtaining a state-per-cycle display of acquired data. Suppressing overfetched instructions may assist in following program execution trace more clearly. Suppressing instructions may be useful if your primary interest is data operand reads and writes.

"Probable overfetch" means states marked with a "*" or "-". "Possible overfetch" means states marked with a "?".

When instructions are suppressed, the overfetch show/suppress controls have no effect.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, memory writes can be shown, with all other operations suppressed, allowing quick analysis of memory writes.

Code Synchronization

The Code Synchronization enables the inverse assembler to resynchronize with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To resynchronize the inverse assembler, use the procedure in "To use the Invasm key".

Display Formats

The enhanced inverse assembler (I603E or I603PE) allows you to configure various aspects of the disassembler display. The configuration options are listed below.

+ Separator Either blanks or commas may be used to separate operands.

```
andis.  r3  r3  F000
andis.  r3,r3,F000
```

The generic disassemblers (I603 and I603P) always use blanks as separators.

+ Numerics Either of two conventions may be selected to display numeric data. The conventions are dense and common.

	dense	common
hex	FFF00230	0xFFF00230
decimal	31.	31
binary	%00100	0b00100

Since most of the numeric data produced by the inverse assembler is hexadecimal, the dense format uses a little less screen space. The generic disassemblers (I603 and I603P) always use dense numerics.

+ Dialect Three mnemonic dialects are available: Raw, Simplified, and Extended. The generic disassemblers (I603 and I603P) always use the Extended dialect.

The Raw dialect provides mnemonics and operands as specified by the PowerPC programming environment, eg the rotate left word immediate then and with mask instruction:

```
rlwinm  r30  r30  16. 16. 31.
```

The Simplified dialect simplifies the operands for the rotate instructions: the rlwinm bit mask is presented as the hex value of the mask generated by the two decimal bit numbers:

```
rlwinm  r30  r30  16. 0000FFFF
```

Additionally, a number of common extensions to PowerPC assembly language are decoded:

Conditional traps and branches decode the condition mnemonically when possible. For some conditions which have no conventional mnemonics (for example, "signed less than or unsigned greater than"), the condition field is displayed in binary.

- The L bit is omitted as a compare operand. Instead, compares are decoded as "cmpw" (or "?cmpd").
- "Add immediate" instructions with a negative immediate operand are decoded as subtract immediate ("subi").
- "Subtract from" instructions subf and subfc are decoded as subtract instructions sub and subc with the operands exchanged so that "sub r3 r4 r5" is mnemonically interpreted as "r3 = r4 - r5."
- ori r0 r0 0000 is decoded as "nop".
- add immediate and add immediate shifted instructions, addi and addis, with a null source register are decoded as load immediate and load immediate shifted, li and lis.
- or instructions with identical source registers are decoded as move register, mr.
- nor instructions with identical source registers are decoded as not register, not.
- xor and eqv instructions with identical source and destination registers are decoded as clear and set, clr and set, respectively.
- the cror, crnor, crxor, and creqv instructions map analogously to crmv, crnot, crclr, and crset.
- when the mtcrf instruction field mask specifies the entire cr, it is decoded as mtcr.

The Extended dialect adds several extended opcodes for the rotate instructions. For example, the function of the rlwinm instruction

```
rlwinm  r30  r30  16. 16. 31.
```

is to shift right word immediate, eg

```
srwi    r30  r30  16.
```

The following listing shows the extended mnemonics for the integer rotate instructions.

Mnemonic	Decoded As	
rlwimi (rotate left word immediate then mask insert)	inslwi insrwi	insert from left immediate insert from right immediate
rlwinm (rotate left word immediate then AND with mask)	rotlwi rotrwi slwi srwi extlwi extrwi clrlwi clrrwi clrlslwi	rotate left immediate rotate right immediate shift left immediate shift right immediate extract and left justify immediate extract and right justify immediate clear left immediate clear right immediate clear left and shift left immediate
rlwnm (rotate left word then AND with mask)	rotlw	rotate left

PowerPC assemblers support a number of extended mnemonics for some popular assembly language instructions as described in the PowerPC 603 User's Manual. The HP E2455A disassembler supports the following extensions of dialect-sensitive instructions.

raw	simplified	extended
bc %00100,2,FFF00230	bne cr0,FFF00230	bne cr0,FFF00230
tw %10000,r5,r6	tw lt,r5,r6	tw lt,r5,r6
cmp cr1,0,r0,r16	cmpw cr1,r0,r16	cmpw cr1,r0,r16
ori r0,r0,0000	nop	nop
addi r6,r6,FCFC	subi r6,r6,0304	subi r6,r6,0304
subf r7,r19,r16	sub r7,r16,r19	sub r7,r16,r19
addi r3,0,7000	li r3,7000	li r3,7000

addis r3,0,7000	lis r3,7000	lis r3,7000
mtcrf %11111111,r5	mtcr r5	mtcr r5
or r4,r5,r5	mr r4,r5	mr r4,r5
nor r4,r5,r5	not r4,r5	not r4,r5
xor r7,r7,r7	clr r7	clr r7
eqv r8,r8,r8	set r8	set r8
creqv 7,7,7	crset 7	crset 7
crxor 8,8,8	crclr 8	crclr 8
cror 7,8,8	crmv 7,8	crmv 7,8
crnor 8,9,9	crnot 8,9	crnot 8,9
rlwnm r8,r7,r6,0,31.	rlwnm r8,r7,r6,FFFFFFFF	rotlw r8,r7,r6
rlwimi r3,r3,24.,8,23.	rlwimi r3,r3,24.,00FFFF00	inslwi r3,r3,16.,8
rlwimi r8,r3,17,8,23.	rlwimi r3,r3,17.,00FE0000	insrwi r8,r3,7,8
rlwinm r6,r4,8,0,14	rlwinm r6,r4,8,0xFFFE0000	extlwi r6,r4,15,8
rlwinm r6,r4,16,24,31	rlwinm r6,r4,16,0x000000FF	extrwi r6,r4,8,8
rlwinm. r6,r4,4,0,31	rlwinm. r6,r4,4,0xFFFFFFFF	rotlwi. r6,r4,4
rlwinm r6,r4,28,0,31	rlwinm r6,r4,4,0xFFFFFFFF	rotrwi r6,r4,4
rlwinm r6,r4,1,0,30	rlwinm r6,r4,1,0xFFFFFFFE	slwi r6,r4,1
rlwinm r6,r4,31,1,31	rlwinm r6,r4,31,0x7FFFFFFF	srwi r6,r4,1
rlwinm r6,r4,0,1,31	rlwinm r6,r4,0,0x7FFFFFFF	clrlwi r6,r4,1
rlwinm r6,r4,0,0,7	rlwinm r6,r4,0,0xFF000000	clrrwi r6,r4,14
rlwinm r6,r4,6,6,25	rlwinm r6,r4,6,0x03FFFC0	clrlslwi r6,r4,12,6

Done Field

When you are finished with the Invasm Options pop-up menu, use the Done key to return to the Listing menu.

Disabling the Instruction Cache

When the instruction cache is enabled, many PowerPC 603 instructions are executed from the cache and do not appear on the external bus. To get an execution trace on the bus, the instruction cache can be disabled. This must be done in supervisor mode.

- Disable the cache with the following code:

```
mfspr   r3  hid0
rlwinm  r3  r3  0  17  15  # clear bit 16 (ICE)
mtspr   hid0  r3
isync
```

- To also disable the data cache use:

```
mfspr   r3  hid0
rlwinm  r3  r3  0  18  15  # clear ICE and DCE
mtspr   hid0  r3
isync
```

- To invalidate and disable the caches use:

```
mfspr   r3  hid0
ori     r3  0C00          # set ICFI and DCFI
mtspr   hid0  r3
rlwinm  r3  r3  0  22  19  # clear ICFI and DCFI
mtspr   hid0  r3
rlwinm  r3  r3  0  18  15  # clear ICE and DCE
mtspr   hid0  r3
isync
```

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the HP2455A hardware including product, electrical, and environmental characteristics, signal mapping, circuit board dimensions, and repair information.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Product Characteristics		
Microcontroller Supported	PowerPC 603	
Package Supported	240-pin PQFP	
Probes Required	8 required for disassembly. 10 available.	
Electrical Characteristics		
Power Requirements	None.	
Signal Line Loading	10pF, 100 kohms on all signals.	
Environmental Characteristics		
Temperature	Operating	0 to + 50 degrees C +32 to +131 degrees F
Altitude	Operating	4,600 m 15,000 feet
Humidity	Up to 75% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.	

Signal-to-Connector Mapping

The following table shows the the preprocessor PGA socket pin mapping.

Table 3-1 **PowerPC 603 Signal List**

Pod	Analyzer Bit	PowerPC 603 Pin #	Signal Name	Analyzer Label	Analyzer Label
J6	CLK1	201	TCK	TCK	
J6	15	204	L1TSTCLK	L1Tclk	
J6	14	203	L2TSTCLK	L2Tclk	
J6	13	218	APE	APE	
J6	12	217	DPE	DPE	
J6	11	225	CSE	CSE	
J6	10	232	RSRV	RSRV-	
J6	9	234	TBEN	TBEN	
J6	8	233	TBLISYNC	TBLISY	
J6	7	38	DP0	DP	
J6	6	40	DP1	DP	
J6	5	41	DP2	DP	
J6	4	42	DP3	DP	
J6	3	46	DP4	DP	
J6	2	47	DP5	DP	
J6	1	48	DP6	DP	
J6	0	50	DP7	DP	

Pod	Analyzer Bit	PowerPC 603 Pin #	Signal Name	Analyzer Label		Analyzer Label
J5	CLK1	180	TT4	TT4		
J5	15	197	TSIZ0	TSIZ		STAT
J5	14	196	TSIZ1	TSIZ		STAT
J5	13	195	TSIZ2	TSIZ		STAT
J5	12	192	TBST	TSIZ	TBST-	STAT
J5	11	191	TT0	Atomic	TT	STAT
J5	10	190	TT1	R/-W	TT	STAT
J5	9	185	TT2	Invldt	TT	STAT
J5	8	184	TT3	A Only	TT	STAT
J5	7	189	SRESET	SRSET-		STAT
J5	6	188	INT	INT-		STAT
J5	5	156	DRTRY	DRTRY-	acks	STAT
J5	4	155	TA	TA-	acks	STAT
J5	3	154	TEA	TEA-		STAT
J5	2	150	XATS	XATS		STAT
J5	1	149	TS	TS		STAT
J5	0	145	DBB	DBB		STAT
J3	CLK1	--				
J3	15	179	A0	ADDR		
J3	14	2	A1	ADDR		
J3	13	178	A2	ADDR		
J3	12	3	A3	ADDR		
J3	11	176	A4	ADDR		
J3	10	5	A5	ADDR		
J3	9	175	A6	ADDR		
J3	8	6	A7	ADDR		
J3	7	174	A8	ADDR		
J3	6	7	A9	ADDR		
J3	5	170	A10	ADDR		
J3	4	11	A11	ADDR		
J3	3	169	A12	ADDR		
J3	2	12	A13	ADDR		
J3	1	168	A14	ADDR		
J3	0	13	A15	ADDR		

Pod	Analyzer Bit	PowerPC 603 Pin #	Signal Name	Analyzer Label	Analyzer Label
J4	CLK1	212	SYSCLK	SYSCLK	
J4	15	166	A16	ADDR	
J4	14	15	A17	ADDR	
J4	13	165	A18	ADDR	
J4	12	16	A19	ADDR	
J4	11	164	A20	ADDR	
J4	10	17	A21	ADDR	
J4	9	160	A22	ADDR	
J4	8	21	A23	ADDR	
J4	7	157	A24	ADDR	
J4	6	22	A25	ADDR	
J4	5	158	A26	ADDR	
J4	4	23	A27	ADDR	
J4	3	151	A28	ADDR	
J4	2	30	A29	ADDR	
J4	1	144	A30	ADDR	
J4	0	37	A31	ADDR	

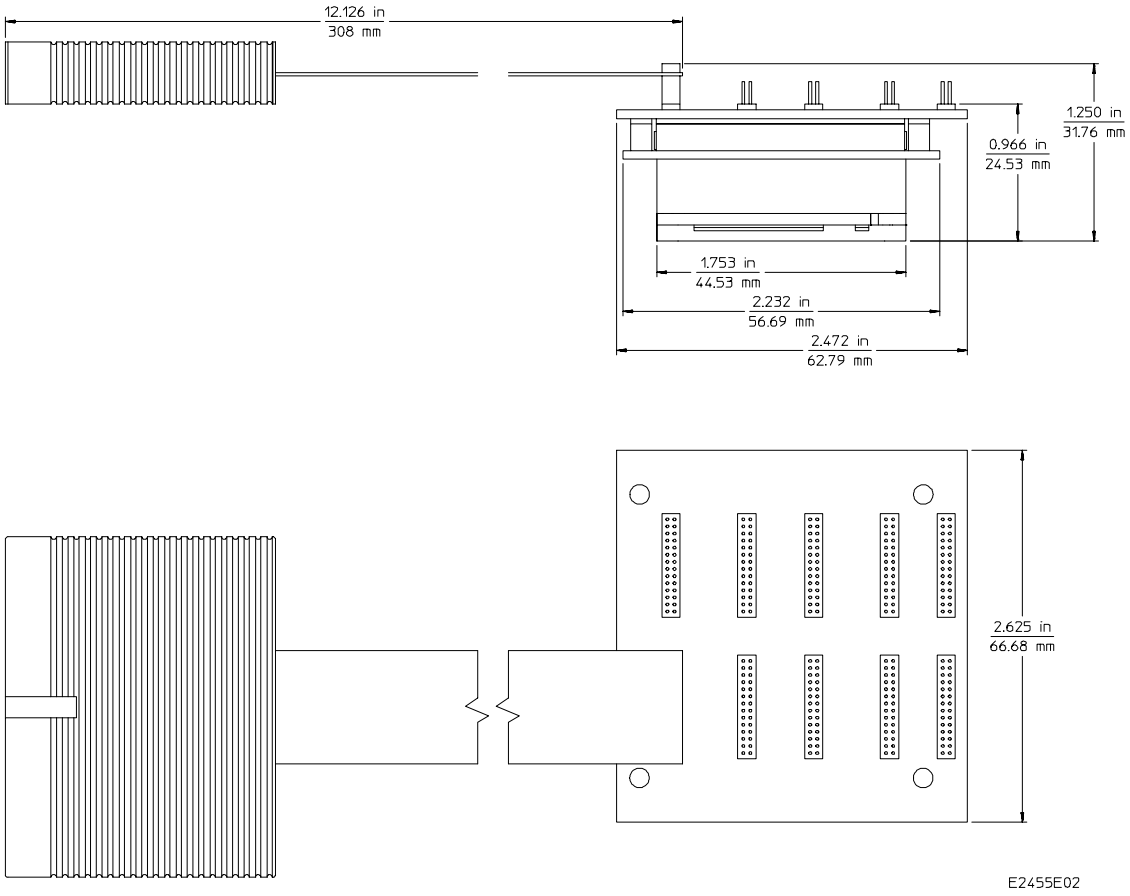
Pod	Analyzer Bit	PowerPC 603 Pin #	Signal Name	Analyzer Label		Analyzer Label
J2	CLK1	235	QACK	QACK-		
J2	15	214	HRESET	HRSET-		STAT
J2	14	215	CKSTP	CKSTP-		STAT
J2	13	216	CHECKSTOP	CHKOUT		STAT
J2	12	219	BR	BR-		STAT
J2	11	224	TC0	TC0	TC	STAT
J2	10	223	TC1	TC1	TC	STAT
J2	9	236	WT	WT-		STAT
J2	8	237	CI	CI-		STAT
J2	7	1	GBL	GBL-		STAT
J2	6	25	DBWO	DBWO-		STAT
J2	5	26	DBG	DBG-		STAT
J2	4	27	BG	BG-		STAT
J2	3	28	AACK	AACK-	acks	STAT
J2	2	31	QREQ	QREQ-		STAT
J2	1	32	ARTRY	ARTRY-	acks	STAT
J2	0	36	ABB	ABB-		STAT
J1	CLK1	221	CLKOUT	CLKOUT		
J1	15	231	AP0	AP		
J1	14	230	AP1	AP		
J1	13	227	AP2	AP		
J1	12	226	AP3	AP		
J1	11	186	MCP	MCP-		
J1	10	187	SMI	SMI-		
J1	9	198	TDO	TDO		
J1	8	200	TMS	TMS		
J1	7	199	TDI	TDI		
J1	6	202	TRST	TRST-		
J1	5	--				
J1	4	205	LSSDMODE	LSSDMO		
J1	3	213	PLLCF0	PLLCFG		
J1	2	211	PLLCF1	PLLCFG		
J1	1	210	PLLCF2	PLLCFG		
J1	0	208	PLLCF3	PLLCFG		

Pod	Analyzer Bit	PowerPC 603 Pin #	Signal Name	Analyzer Label	Analyzer Label
J8	CLK1				
J8	15	117	DL16	DATA_B	
J8	14	107	DL17	DATA_B	
J8	13	106	DL18	DATA_B	
J8	12	105	DL19	DATA_B	
J8	11	102	DL20	DATA_B	
J8	10	101	DL21	DATA_B	
J8	9	100	DL22	DATA_B	
J8	8	51	DL23	DATA_B	
J8	7	52	DL24	DATA_B	
J8	6	55	DL25	DATA_B	
J8	5	56	DL26	DATA_B	
J8	4	57	DL27	DATA_B	
J8	3	58	DL28	DATA_B	
J8	2	62	DL29	DATA_B	
J8	1	63	DL30	DATA_B	
J8	0	64	DL31	DATA_B	
J7	CLK1				
J7	15	85	DH16	DATA	
J7	14	84	DH17	DATA	
J7	13	83	DH18	DATA	
J7	12	82	DH19	DATA	
J7	11	81	DH20	DATA	
J7	10	80	DH21	DATA	
J7	9	78	DH22	DATA	
J7	8	76	DH23	DATA	
J7	7	75	DH24	DATA	
J7	6	74	DH25	DATA	
J7	5	73	DH26	DATA	
J7	4	72	DH27	DATA	
J7	3	71	DH28	DATA	
J7	2	68	DH29	DATA	
J7	1	67	DH30	DATA	
J7	0	66	DH31	DATA	

Pod	Analyzer Bit	PowerPC 603 Pin #	Signal Name	Analyzer Label	Analyzer Label
J9	CLK1	--			
J9	15	115	DH0	DATA	
J9	14	114	DH1	DATA	
J9	13	113	DH2	DATA	
J9	12	110	DH3	DATA	
J9	11	109	DH4	DATA	
J9	10	108	DH5	DATA	
J9	9	99	DH6	DATA	
J9	8	98	DH7	DATA	
J9	7	97	DH8	DATA	
J9	6	94	DH9	DATA	
J9	5	93	DH10	DATA	
J9	4	92	DH11	DATA	
J9	3	91	DH12	DATA	
J9	2	90	DH13	DATA	
J9	1	89	DH14	DATA	
J9	0	87	DH15	DATA	
J10	CLK1	153	DBDIS	DBDIS-	
J10	15	143	DL0	DATA_B	
J10	14	141	DL1	DATA_B	
J10	13	140	DL2	DATA_B	
J10	12	139	DL3	DATA_B	
J10	11	135	DL4	DATA_B	
J10	10	134	DL5	DATA_B	
J10	9	133	DL6	DATA_B	
J10	8	131	DL7	DATA_B	
J10	7	130	DL8	DATA_B	
J10	6	129	DL9	DATA_B	
J10	5	126	DL10	DATA_B	
J10	4	125	DL11	DATA_B	
J10	3	124	DL12	DATA_B	
J10	2	123	DL13	DATA_B	
J10	1	119	DL14	DATA_B	
J10	0	118	DL15	DATA_B	

Circuit Board Dimensions

The following figure gives the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.



Circuit Board Dimension Diagram

Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

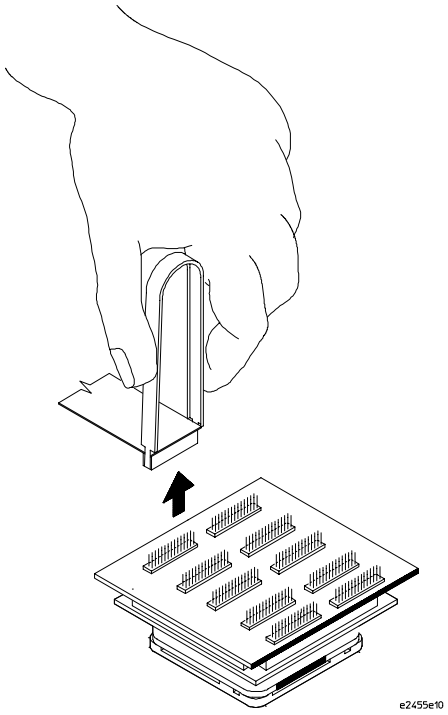
Table 3-2 Replaceable Parts

HP Part Number	Description
16550-63201	Flexible Cable Assembly
E5315A	PQFP Adapter
E2455-66501	PowerPC 603 Interface Card
5041-9489	Locator kit with inserts
5041-9490	Locator kit with no inserts

Flexible Cable Removal

If you ever need to remove the flexible cable assemblies from the interface card, use the DIP Extracter tool provided.

1 Use the DIP Extracter tool as shown to remove flexible cable assemblies from the interface card.



Flexible Cable Removal Diagram

2 Ensure correct orientation and alignment when reinstalling the cable assemblies.

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